CLAIMS

1. A method of making a microelectronic assembly, comprising:

a) providing a microelectronic element having a first major surface with protrusions projecting from the first major surface;

b) covering the first major surface and the protrusions with a material;

c) removing a portion of the material so that portions of the protrusions are accessible; and

d) assembling the microelectronic element with a microelectronic component.

2. The method of claim 1, wherein the protrusions comprise bumps of bonding material.

3. The method of claim 2, wherein the protrusions comprise a solder selected from the group consisting of high lead solder, C4 solder and eutectic solder.

4. The method of claim 1, wherein the material comprises an epoxy.

5. The method of claim 1, wherein the material has a low coefficient of thermal expansion.

6. The method of claim 1, wherein the protrusions project from the material a distance of about 50 μm or less.

7. The method of claim 1, wherein the step of covering the first major surface and the protrusions comprises:

a) disposing the microelectronic element in the recess of a mold tool so that the first major surface is disposed in the recess; and

b) disposing the material in the recess so as to cover the first major surface.

8. The method of claim 7, wherein the recess is defined by a base, a wall extending from the base, and an open side.

9. The method of claim 8, wherein the mold tool has at least one protruding member extending from the base into the recess, the at least one protruding member being spaced from the wall.

10. The method of claim 9, wherein the at least one protruding member defines an inner region within the recess and the first major surface is disposed in the inner region.

11. The method of claim 10, wherein the material is disposed in the recess so that the first major surface and the protrusions are covered by the material.

12. The method of claim 11, wherein the material is disposed in the recess so that, after removing the mold tool, the at least one protruding member leaves at least one groove in the material.

13. The method of claim 1, wherein the material is applied to the first major surface as a flowable, curable material and cured to a relatively rigid material.

14. The method of claim 1, wherein the portion of the material is removed by grinding.

15. The method of claim 1, wherein the portion of the material is removed by etching.

16. The method of claim 1, wherein the step of removing a portion of the material includes removing a portion of the protrusions.

17. The method of claim 16, wherein the step of removing a portion of the material forms a surface of material incorporating at least one surface of the protrusions.

18. The method of claim 17, wherein the step of removing a portion of the material comprises removing a portion of the material so that portions of the protrusions project from the material and further comprising removing the portions of the protrusions.

19. The method of claim 1, further comprising interconnecting the protrusions of the microelectronic element with conductive elements of the microelectronic component.

20. The method of claim 19, wherein the microelectronic component comprises a base layer and the conductive elements comprise leads, each of the leads having a first end and a second end.

21. The method of claim 20, wherein the first ends of the leads are connected to the microelectronic component adjacent a lower surface of the base layer.

22. The method of claim 21, wherein the step of interconnecting comprises bonding the second ends of the leads to the protrusions of the microelectronic element.

23. The method of claim 22, further comprising deforming the leads so that the leads extend between the microelectronic component and the microelectronic element.

24. The method of claim 23, further comprising forming a dielectric layer extending between the microelectronic component and the microelectronic element so that the leads are embedded in the dielectric layer.

25. The method of claim 24, wherein the step of forming a dielectric layer includes introducing a flowable material between the microelectronic component and the microelectronic element.

26. The method of claim 24, wherein the coefficient of thermal expansion for the molding material is closer in value to the coefficient of thermal expansion of the microelectronic element than the coefficient of thermal expansion for the dielectric layer.

27. The method of claim 20, wherein the microelectronic component has conductive elements comprising leads, and further comprising deforming the leads so that the leads are brought into engagement with the protrusions.

28. The method of claim 1, further comprising:

a) connecting the protrusions to conductive elements of the microelectronic component; and

b) forming a dielectric layer over the first major surface so as to surround the conductive elements.

29. The method of claim 28, wherein the coefficient of thermal expansion of the material is closer in value to the coefficient of thermal expansion of the microelectronic element than the coefficient of thermal expansion of the dielectric layer.

30. A method of forming protrusions on a microelectronic element, comprising:

a) providing a semiconductor chip having a first major surface and contacts exposed at the first major surface; and

b) forming protrusions including applying a first conductive layer over the contacts, and a second conductive layer on the first conductive layer;

c) wherein the protrusions project 50 μm or less from the first major surface.

31. The method of claim 30, wherein at least one of the first conductive layer and second conductive layer comprises bonding material.

32. The method of claim 31, wherein the first conductive layer comprises a high lead solder and the second conductive layer comprises eutectic solder.

33. The method of claim 32, wherein the first conductive layer has a height between about 5 μm and about 25 μm and the second conductive layer has a height between about 10 μm and about 25 μm.

34. The method of claim 33, wherein the first conductive layer comprises an alloy including lead and tin.

35. The method of claim 34, wherein the step of applying a second conductive layer comprises dipping.

36. The method of claim 34, including applying a third conductive layer on the second conductive layer.

37. The method of claim 36, wherein the first conductive layer comprises a high lead solder, the second conductive layer comprises lead and the third conductive layer comprises tin.

38. The method of claim 37, further comprising reflowing the first conductive layer, second conductive layer and third conductive layer to form a protrusion having a core and an outer layer, the core comprising a high lead alloy and the outer layer comprising an eutectic layer.

39. The method of claim 30, further comprising applying an initial layer on at least a portion of the first major surface so that the initial layer is in contact with the contacts, before the step of applying the first conductive layer.

40. The method of claim 39, wherein the initial layer comprises at least one metal selected from the group consisting of chromium, copper, titanium, nickel, gold, and alloys of chromium, copper, titanium, nickel and gold.

41. A method of forming a microelectronic chip package, comprising the method of forming protrusions according to claim 30, further comprising providing a connection component having conductive elements, interconnecting the protrusions with the conductive elements, and forming a dielectric layer extending between the microelectronic component and the microelectronic element so that the protrusions and the conductive elements are at least partially embedded in the dielectric layer.

42. A semiconductor chip assembly, comprising:

a) a semiconductor chip having a first major surface and protrusions projecting from the first major surface a distance of less than about 50 μm; and

b) a dielectric layer overlying the first major surface and having conductive elements extending through the dielectric layer and being connected to the protrusions.

43. The assembly of claim 42, wherein the dielectric layer comprises a compliant material.

44. The assembly of claim 42, wherein the conductive elements comprise leads.

45. The assembly of claim 44, wherein the assembly includes a molding material overlying the semiconductor chip and forming the first major surface.

46. The assembly of claim 45, wherein the coefficient of thermal expansion of the material is closer in value to the coefficient of thermal expansion of the semiconductor chip

than the coefficient of thermal expansion of the dielectric layer.

47. The assembly of claim 42, wherein the dielectric layer has a thickness of between about 100 μm and about 200 μm.

48. The assembly of claim 47, wherein the projections project from the first major surface a distance between about 10 μm and about 50 μm.

49. The assembly of claim 42, further comprising a base layer overlying the dielectric layer and forming an upper surface of the package.

50. The assembly of claim 45, wherein the material has grooves lying outwardly of peripheral edges of the semiconductor chip.

51. The assembly of claim 42, wherein the protrusions have a core and an outer layer, the core comprising a high lead alloy and the outer layer comprising a eutectic layer.

52. The assembly of claim 42, wherein the protrusions comprise a solder selected from the group consisting of high lead solder, C4 solder and eutectic solder.